DC Arc Hazard Mitigation Design at a Nuclear Research Facility

Walter P. Mendenhall, PE
Senior Member, IEEE
Wiley | Wilson, 127 Nationwide Drive, Lynchburg, VA 24502
wmendenhall@wileywilson.com

Though potential arc heat and blast energy from dc sources may be significant, the risk assessment for exposure to dc energy sources is often not performed because the requirement to do so is not understood. Making the task of quantifying dc arc energies more intimidating is that the professional engineer often assumes liability for any errors or omissions that may result in injury — or worse. Compounding the issue even further is that the analysis work is often based on tools, methods, and verifications for dc arc heat and blast energies that are incomplete and immature.

Explained here is one approach taken to perform an arc heat and blast analysis for a research facility, specifically a concentrated load supplied by eight 1 MW SCR rectifiers regulating +/-300 Vdc outputs to tightly arranged terminations at a load. During the course of the research, the connections were to be reconfigured, followed by a planned retuning of the regulated dc output using hand-held multi-meters at the load terminations, without wearing PPE. After assessing the risk, the research engineers were easily convinced that a full analysis needed to be performed with risk mitigation design.

Index Terms — arc flash analysis, dc arc, dc arc hazard, mitigation

I. INTRODUCTION

The arc hazard from ac electrical systems has become well known over the past decade thanks in large part to the widespread application and enforcement of NFPA 70E, the *Standard for Electrical Safety in the Workplace®*. NFPA 70E was developed using several incident energy quantification methods. One of these, included in its annex, is IEEE 1584, "Guide for Performing Arc-Flash Hazard Calculations." Until now a validated method of calculating the arc hazard from dc sources has been conspicuously missing from this standard. Therefore, dc arc flash hazard has been estimated at best and ignored at worst, which leaves electrical workers under-protected.

NFPA 70E – 2012, Annex D.8, includes a validated, conservative method for computing incident energy from dc arc flash where the available dc bolted fault current is known. Quantified warning labels for equipment can now be provided, where workers are exposed to live dc so that the appropriate personal protective equipment (PPE) can be worn. It is anticipated that OSHA and state safety agencies will soon enforce compliance of arc flash responsibilities for dc equipment as they have for ac.

The emergence of a method to determine dc arc flash hazard is a significant step forward. Unfortunately, the developments of dc arc flash software tools and dc short circuit analysis tools that are fully integrated with ac tools lags behind the new standard. This gap presents challenges to engineers but also represents an opportunity for manufacturers to introduce tools and software that can fill this need.

Until such items are introduced, however, it is necessary for engineers to use other methods to determine dc arc flash hazards. This summary is an example of a process that was used to evaluate dc arc hazard for multiple rectifiers supplying an array of resistive loads. The purpose is to encourage others to recognize dc arc hazards and to suggest resources that may be helpful to those involved in electrical systems hazard analysis.

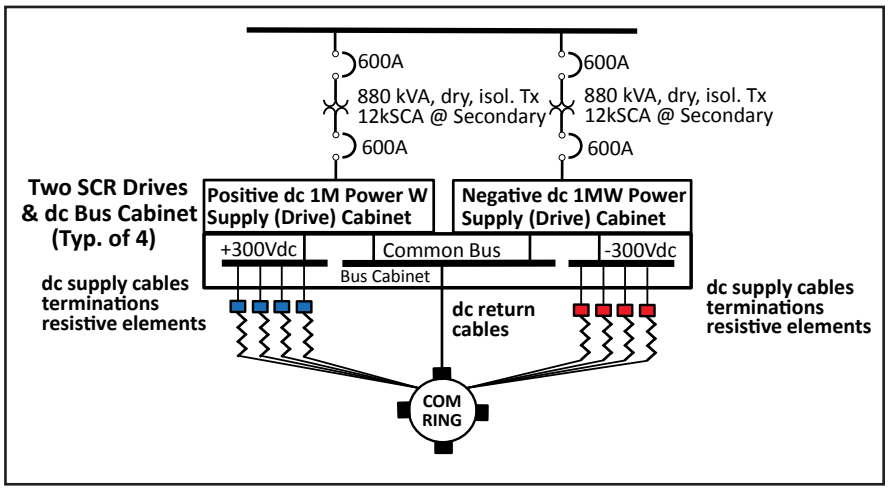

Figure 1. DC Arc Hazards

978-1-4799-2098-3/14/$31.00 ©2013 IEEE

II. EVALUATING DC ARC HAZARDS FROM RECTIFIERS

This project involved architecture and engineering services for the design and construction of a nuclear research facility. The work included an arc flash hazard analysis for the ac electrical system components that were to be installed. The system included eight 1050 HP dc drives with SCRs to regulate their variable outputs to a nominal 300 Vdc, which originally was not part of the scope of analysis. The drives supplied 300 Vdc resistive heater loads that could generate nearly 1.4 MW of heat. Because personnel, contractors, and vendors would be exposed to live dc voltages during commissioning and startup system testing, the project included analyzing the dc system arc hazard.

Models of the electrical system were built in a widely used electrical system analysis tool, but the short circuit analyses for the ac and dc portions of the electrical system had to be performed separately due to the lack of integration between these tools. For instance, the software model for rectifiers required manual entry for values of the ac source system impedance and available fault energy into the component editor dialog box. Therefore, if the input parameters changed due to reconfiguration of the ac system, any updated values from the ac short circuit analysis results had to be found and copied into the dc system analysis application manually. With multiple rectifiers in the system, each with different length of supply conductors, iterations of this process quickly became labor intensive and subject to errors.

A. *Solving the dc Fault Current Problem*

The first step in computing the dc arc hazard is to determine the available current at the fault. The dc system is composed of eight dc drives, each with a rated input of 690 Vac and rated output of 1410 A at 750 Vdc. This rating was used to determine the "effective impedance" of the rectifier [1]. The eight drive outputs were configured as four pairs of plus and minus supplies to four bus cabinets collocated with each pair of drives. The controllers were programmed to respond to a remote master controller to supply a variable voltage regulated output centered about a nominal +/- 300 Vdc. Highly stranded flexible cables were routed in trays distributing the dc power to an array of resistive elements. Initially, half of these elements were terminated with +300 Vdc and an adjacent element termination of -300 Vdc was located only a few inches away. All of the elements had common returns to the associated bus through the tray cabling. With the array as originally constructed, the alternating plus and minus terminations of the resistors with rows of similarly alternating terminations immediately above and below, supplied by the other three pairs of dc drives could easily produce a high-energy cascading failure.

The objective was to develop a documented standard method to compute a fault value for the exposed terminations of the core simulator heater resistors, the buses in the dc distribution enclosure, and the output terminations of the rectifiers (drives). It was decided to evaluate the outputs of dc fault currents from existing dc system analysis software [1] against values obtained from manual spreadsheet calculations based on ANSI [2] and IEC [3] methods. [a] Initial discussions with the analysis software vendors at the time indicated that several companies were in the process of developing dc arc hazard analysis tools; unfortunately, they were not available until after this project was completed. Because there were some unanswered questions about the meanings of some of the available beta version tool's dialog entries, manual calculations of the dc fault current were performed based on the IEC Standard 61660-1 [3] method. The referenced work by J.C. Das [4] provides an example of this method.

B. *Calculations Used During the Process*

The peak short circuit current i_{1pD} was computed with:

$$i_{1pD} = \kappa_D I_{kD} \tag{1}$$

where constant κ_D was calculated by the equation from [3]:

$$\kappa_D = 1 + \frac{2}{\pi} e^{-\left(\frac{\pi}{3}+\varphi_D\right)\cot\phi_D} \sin\phi_D \left(\frac{\pi}{2} - \arctan\frac{L_{DBr}}{L_N} \right) \tag{2}$$

where

L_{DBr} is the inductance on the load side of the rectifier

L_N is the inductance on the line side and

I_{kD} is the quasi steady-state current is defined in terms of equivalent circuit diagram of the rectifier defining parameters used in multiple defining equations (8) through (13) in [3].

The rise time constant τ_{1D} was calculated from:

$$\tau_{1D} = \left[2 + \left(\kappa_D - 0.9\right)\left(2.5 + 9\frac{L_{DBr}}{L_N} \right) \right] ms \tag{3}$$

and the decay time constant τ_{2D} from:

$$\tau_{2D} = \frac{2}{\frac{R_N}{X_N}\left(0.6 + 0.9\frac{R_{DBr}}{R_N} \right)} ms \tag{4}$$

The variables in these equations in this summary are documented in [3] and [4].

978-1-4799-2098-3/14/$31.00 ©2013 IEEE

Published parameters for resistive and inductive impedances of dc conductors were not readily available from vendors, which also explained why dc conductors were not found in the vendor's software library. Only typical values for relatively low strand count conductors were found in sources like the *Standard Handbook for Electrical Engineers* [5]. Only through verbal contact with vendor engineers was this information gathered.

The fault current formula was tested for sensitivity to the minimum and maximum variations in conductor lengths used in the distribution of ac to each of the eight power supply rectifiers as well as within the dc distribution to the bus enclosure and resistors. Because conductors were fairly large and the lengths short, there was no significant variation in results so an average length was used.

There were no dc protective devices in this system so the calculated peak current and rise and fall time duration was plotted on time-current curves for the upstream electronic trip circuit breaker and the current limiting URS fuses on three-phase 480Vac (source) side of the rectifiers for each of the three fault locations. In each case, the magnitude and duration of the peak fault current was insufficient to part the fuse before the breaker opened. Therefore the quasi-steady state value for dc fault current was used to determine an equivalent ac fault current to determine the trip delay time needed to compute incident arc energy.

C. *Converting dc Fault Current into Incident Energy*

In his recent paper on arc flash energy conversion of dc faults [6], Dan Doan developed the following formula for incident energy:

$$IE_{\max\ power} = 0.005\left(\frac{V_{sys}^{\ 2}}{R_{sys}}\right)\frac{T_{arc}}{D^2} \qquad (5)$$

where

$IE_{\max\ power}$	estimated incident energy at maximum power point (in cal/cm2);
V_{sys}	system voltage (in volts);
R_{sys}	system resistance (in ohms);
T_{arc}	arcing time (in seconds); and
D	distance from arc (in centimeters)

The formula has been validated by several years of empirical measurements made of dc arcs [7].

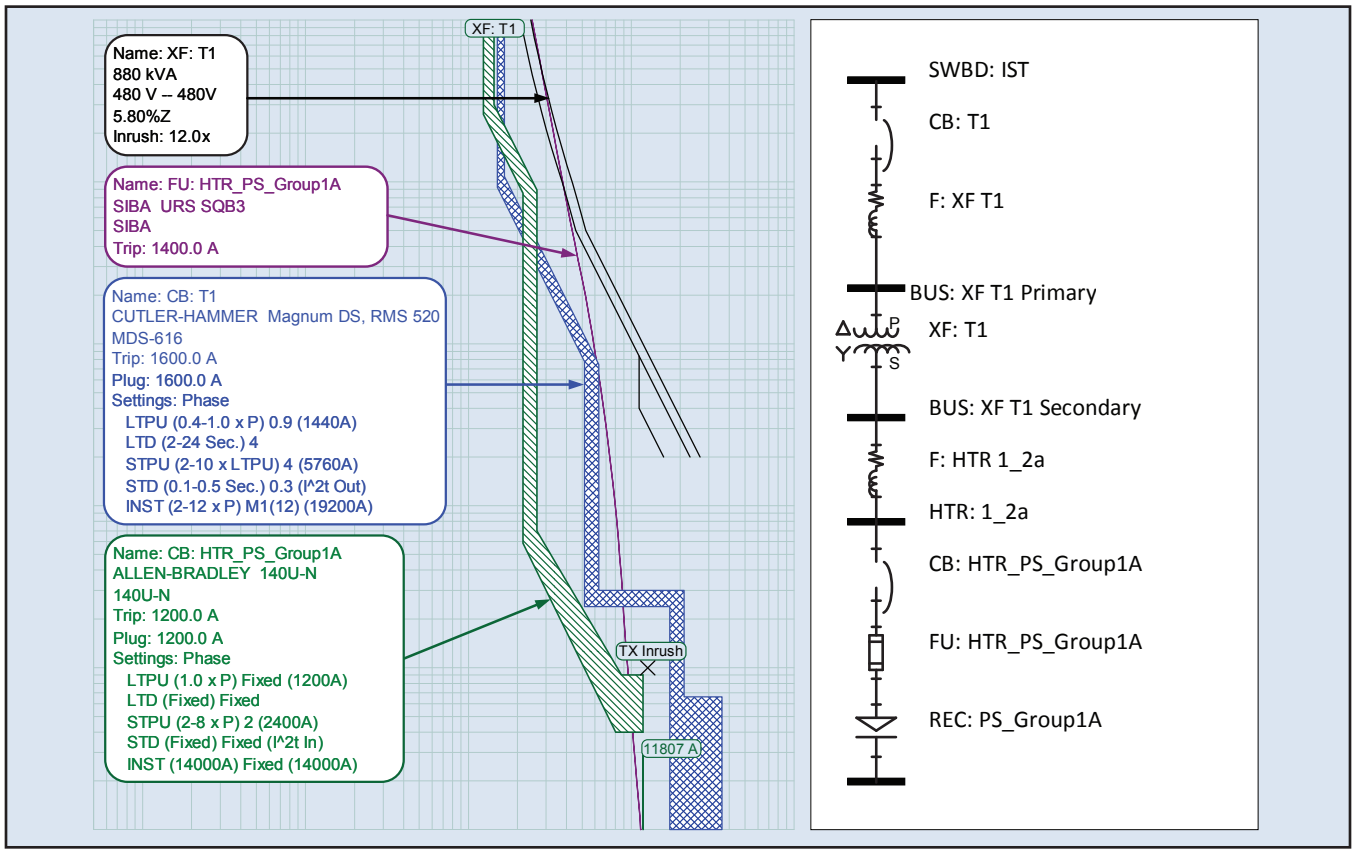

Fig. 2. Time Current Characteristics for DC Power Supply Protective Devices

978-1-4799-2098-3/14/$31.00 ©2013 IEEE

D. *Single Fault Results*

By applying (5) to the system voltage, system resistance, and arc duration at an arm's length working distance of 46 cm (18 in), the incident energy was calculated and the results are shown in Table 1.

Table 1. System DC Arc Hazard Results

Bus Name	Prot Dev Name	Equiv SCac (kA)	Trip Delay (sec)	Incident Energy @ 46cm (cal/cm2)	Arc Flash Boundary cm (in)
Rectifier Output	CB: HTR_PS	2.45	0.601	18.20	178 (70)
Heater Dist Bus	CB: HTR_PS	2.45	0.606	17.79	175 (69)
Heater	CB: HTR_PS	2.43	0.633	8.61	135 (53)

E. *Cascading Fault Results*

Because of the high possibility of a fault at one of the resistor terminations cascading to adjacent terminations, the calculation was performed for the vectorial contribution of adjacent faults up to the maximum for contributions from all four pairs of rectifiers. A spreadsheet was set up to determine the maximum heat and pressure contribution from cascaded arc faults on the surface sphere with an initial radius of 18 inches beyond the initiating arc. The calculations considered the geometry occluding some of the terminations and that the initial arc would reduce the energy of cascaded arc energy supplied from the same pair of rectifiers. The results of worst-case scenarios were well in excess of 40 cal/cm2 for heat energy.

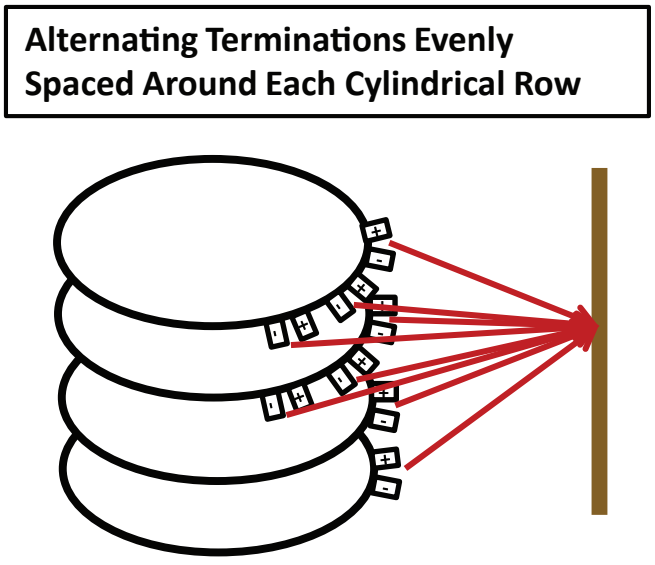

Fig. 3. Cascaded Arc Energy

F. *System and Procedures Redesigned to Reduce Arc* Hazard

This study caused immediate and significant changes in the planned procedures for testing and commissioning the dc system. As a result, measurements were taken with remote sensors rather than handheld meters. Because the terminals of the resistors are not enclosed and subject to exposure, water leakage, and thermal cycling, an unexpected fault could occur exposing unprotected personnel within the area to arc flash hazard. This led to discussions of the design for an effective protective barrier surrounding these terminations.

The barrier design objectives were to achieve safety from arc heat and blast pressures immediately outside the barrier and had to be flexible enough to be disassembled for resistor reconfigurations and routine maintenance when the equipment was powered down. Because of the space constraints, arc suppression blankets supported by steel frameworks were initially proposed as a shield design. However, the intensity and duration of the cascaded fault heat energy at a distance of 14cm (5.5 inches) was greater than 250 cal/cm2 — well beyond the capabilities of available validated multilayer glass and ballistic-fiber blankets at the distance from the arc fault. This meant that additional arc fault energy reductions were needed to ensure the blanket was not compromised by the arc blast heat or pressure.

Reducing the arc energy by reducing fault clearing time of the ac protective devices was not practical without increased nuisance trips or preconditioning fuses. Space limitations of the system prevented the design from incorporating protective devices on the dc side of the rectifier. Changing the physical configuration of the resistor terminations from alternating the plus and minus 300 Vdc terminations for each resistor pair to a new layout with all plus 300 Vdc resistors on one side of an electrical barrier material and all minus 300 Vdc resistors on the other side reduced the driving arc voltage to 300V (+ or – to ground). Both arc heat and blast pressures are directly proportional to the square of the voltage so the heat and pressure were reduced by a factor of four.

Since arc heat and blast pressures are inversely proportional to the square of the distance from the initiating arc to the proposed shield blanket, doubling the distance to 28cm (11 inches) reduced the arc heat to a maximum of 44 cal/cm2 — well within the validated testing of the seven layer arc suppression blanket. The customized blanket was suspended by carabiner clips through grommets to a steel structure and the lower portion of the blanket was cinched by straps below the resistor array structure; thus it would deflect an arc blast upward without rupturing and would be flexible enough to maneuver for maintenance activities. The equipment space where the resistors are located is no longer required to be restricted to access during operation due to arc flash hazard.

978-1-4799-2098-3/14/$31.00 ©2013 IEEE

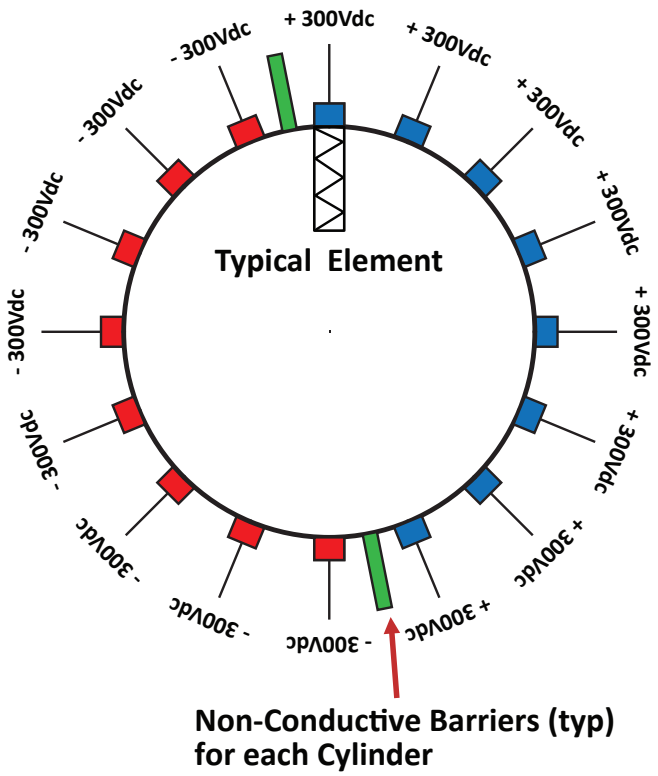

Fig. 4. Rearranged Load Termination Arrangement

APPENDIX A: DC FAULT CURRENT VERIFICATION TESTING

As this paper was written, specifications are being considered to test an exemplar rectifier for a bolted fault at the output terminals. If such a test is made, instrumentation for fault currents and voltages can be made that can be used to verify the computations for this specific model. The effects of overcurrent protection algorithms in the control software may limit the duration of the fault to significantly less than 0.6 second required to trip the breaker with the given source system impedances.[b]

[a] The power systems analysis application provider's "ANSI method" of dc fault current calculation resulted in a higher current with less clearing time for the fault. Without compelling rationale for the different results, the conservative position was to assume the higher dc arc energy derived from the IEC method of dc fault current calculations.

[b] The presence of an overcurrent limiting function in the control software for the rectifier may significantly reduce the exposure to dc arc flash hazard for this system. However, there are numerous letters of interpretation for OHSA's 29 CFR 1910.147, "The control of hazardous energy (lockout/tagout)," [8] that directly state that control hardware and software are NOT normally considered effective, positive forms of isolating hazardous energy.

REFERENCES

[1] DC Short Circuit (ANSI) Reference Manual, SKM Power Tools for Windows™ DC Systems Analysis, Version 6.5.2.6 (Build 3), 2011 Help Document Library.

[2] IEEE 946, *DC Auxiliary Power Systems for Generating Stations*, 1992, Standard 946.

[3] IEC, Short-Circuit Currents in DC Auxiliary Installations in Power Plants and Substations - Part 1: Calculation of short-circuit currents. Standard BS EN 61660-1:1997, incorporating corrigenda March 1999 and March 2000.

[4] J.C. Das, *Power System Analysis: Short Circuit, Load Flow, and Harmonics*, p. 321-322, CRC Press, (2008).

[5] D. G. Fink and H. W. Beaty, *Standard Handbook for Electrical Engineers, 12th Edition*, Section 4, McGraw Hill, (1987).

[6] D. R. Doan, "Arc Flash Calculations for Exposures to DC Systems", *IEEE Transactions on Industry Applications, Vol. 46, No. 6, November/December 2010*.

[7] DC Arc Hazard Assessment Phase II Copyright Material Kinectrics, Inc. Report No. K-012623-RA-0002-R00.

[8] US Department of Labor, 29 CFR 1910.147, Standard Interpretation to Mr. Earl Reyes, January 25, 2008.

978-1-4799-2098-3/14/$31.00 ©2013 IEEE